ABSTRACT OF THE DISCLOSURE

On-chip decoupling capacitor structures, and methods of fabricating such decoupling capacitors are disclosed. On-chip decoupling capacitors help to reduce or prevent L di/dt voltage droop on the power grid for high surge current conditions. The inclusion of one or more decoupling capacitors on a chip, in close proximity to the power grid conductors reduces parasitic inductance and thereby provides improved decoupling performance with respect to high frequency noise. In one embodiment of the present invention, a capacitor stack structure is inserted between metal interconnect layers. Such a capacitor stack may consist of a bottom electrode/barrier; a thin dielectric material having a high dielectric constant; and a top electrode/barrier. In an alternative embodiment, the bottom electrode and/or bottom metal interconnect layer have three dimensional texture to increase the surface area of the capacitor. An illustrative method embodying the present invention, includes fabricating the on-chip decoupling capacitor stack structure and electrically connecting the capacitor to provide efficient capacitive de-coupling. In order to facilitate the removal of photoresist by an oxygen plasma process prior to exposing copper conductors during the capacitor stack etch, an Al hardmask can be used to protect the capacitor formed with Ta_2O_5 dielectric, or a W hardmask can be used to protect the capacitor formed with BST dielectric.